

REMARKS

I. Claims Rejected Under 35 U.S.C. §103(a)

The Examiner rejected claims 23-35 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent 4,609,825 Berger et al. (*Berger*), in view of U.S. Patent Publication No. 2003/0193597 A1 Fossum et al. (*Fossum*), and in further view of U.S. Patent 4,709,259 Suzuki (*Suzuki*) and U.S. Patent 5,541,645 Davis (*Davis*). Applicants respectfully traverse this rejection.

Regarding claim 23, none of the references used by the Examiner discloses the use of two reset bits to operate the reset and wordline shift registers so that the first and second reset bits and the read bit shift through their respective registers while an image frame is being captured, with the first reset bit being one or more rows ahead of the read bit to mark the start of integration, and the second reset bit to generate a correlated double sampling pixel reset value after each pixel integrated intensity value. The Examiner also argues *Suzuki* discloses in Fig. 3 the use of using a second reset bit to vary integration time. However, Applicants maintain a global reset is used to read the integration times for each color in *Suzuki*, hence *Suzuki* does not teach Applicants' claimed use of two reset bits in this regard. The Examiner has pointed to no reference teaching or suggesting the use of two reset bits to operate the reset and wordline shift registers with the first reset bit to mark the start of integration and the second reset bit to generate a correlated double sampling pixel reset value. Absent such teaching or suggestion of this feature of Applicants' claim, the Examiner has failed to satisfy the obligation to make out a *prima facie* case of obviousness as required by the rules of patent examination. In view of this failing of the combination of references, Applicants respectfully submit that the rejection of Claim 23 be withdrawn.

As to claims 24-26, those claims depend directly or indirectly upon claim 23, and are patentable for at least the reasons discussed in support of their base claim. The Examiner is requested to withdraw these rejections as well.

As to independent claims 27 and 31, those claims also require that the use of two reset bits to operate the reset and wordline shift registers. As previously argued, none of the references disclose the use of two reset bits to operate the reset and wordline shift

registers with the first reset bit to mark the start of integration and the second reset bit to generate a correlated double sampling pixel reset value. Therefore, Applicants respectfully request that the rejection of claims 27 and 31 be withdrawn.

Similarly, as to claims 28-30 and 32, those claims depend directly or indirectly upon claim 27 or claim 31, and are patentable for at least the reasons discussed in support of their base claim. Claims 33-37 have been canceled so the rejections are moot. The Examiner is requested to withdraw these rejections as well.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 23-32, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

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Dated: July 13, 2005

By 
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on July 13, 2005.


Margaux Rodriguez July 13, 2005